IN THE CLAIMS

Please amend the claims as follows.

1-26. (Canceled)

27. (Currently Amended) A multi-port buffer, comprising:

a plurality of buffer units, each including

its own memory having a write block and a read block,

its own dedicated port input logic,

its own dedicated port output logic ;

at least one multiplexor, including

an output coupled to the ~~read~~ write block of one of the buffer units,

a first input coupled to the port input logic of the one buffer unit,

a second input coupled to the ~~write~~ read block of another of the buffer units;

flow-control logic to switch the multiplexor between its first and second inputs.

28. (Previously Presented) The buffer of claim 27 further including at least another multiplexor, including

an output coupled to the write block of the other buffer unit,

a first input coupled to the port input logic of the other buffer unit,

a second input coupled to the read block of a further of the buffer units;

29. (Previously Presented) The buffer of claim 27 further including a plurality of multiplexors, each including

an output coupled to the write block of a different one of the buffer units,

a first input coupled to the port input logic of the different one buffer unit,

a second input coupled to the read block of a further of the buffer units;

30. (Currently Amended) The buffer of claim 29 where at least some of the multiplexors have further inputs coupled to the memory ~~units~~ of additional ones of the buffer units

31. (Previously Presented) The buffer of claim 27 where the buffer memories are physically discrete.

32 (Previously Presented) The buffer of claim 27 further including a cross-bar switch coupled between the memory and the port output logic of at least some of the buffer units.

33. (Currently Amended) The buffer of claim 32 where the cross-bar switch can be programmed to send data from the memory ~~unit~~ of any of the some buffer units to the port output logic of any of the some buffer units..

34. (Previously Presented) The buffer of claim 27 where at least one of the buffer units includes write logic coupled between the multiplexor and the memory.

35. (Previously Presented) The buffer of claim 34 where the write logic indicates how much space remains in the memory of its associated buffer unit.

36. (Previously Presented) The buffer of claim 27 where the flow-control logic is adapted to send commands to the port output logics.

37. (Currently Amended) A system, comprising:

a host system;

a plurality of channels to communicate data to a network;

a channel adapter including a multi-port buffer, the buffer comprising

a plurality of buffer units, each including

its own memory having a write block and a read block,

its own dedicated port input logic,

its own dedicated port output logic ;

at least one multiplexor, including

an output coupled to the memory ~~unit~~ of one of the buffer units,

a first input coupled to the port input logic of the one buffer unit,

a second input coupled to the memory ~~unit~~ of another of the buffer units;

flow-control logic to switch the multiplexor between its first and second inputs.

38. (Previously Presented) The system of claim 37 further comprising a multi-stage switch coupled to the channel adapter.

39. (Previously Presented) The system of claim 38 further comprising a central network manager to control the network.

40. (Previously Presented) The system of claim 38 further comprising a plurality of terminal control adapters coupled to the multi-stage switch.

41. (Previously Presented) The system of claim 40 where one of the terminal control adapters couples to a further network.

42. (Previously Presented) The system of claim 37 where the network follows the NGIO protocol.

43. (Currently Amended) A method, comprising:

transmitting data from a first port input to a first buffer memory associated with ~~that~~ the first port input and thence to a first port output;

disabling transmitting data from a second port input to a second buffer memory associated with ~~that~~ the second port input;

thereafter, switching data from an output of the first buffer memory to an input of the second buffer memory, and coupling an output of the second buffer memory to the first port output.

44. (Currently Amended) The method of claim 43 further comprising:

disabling transmitting data from at least a third port input to at least a third buffer memory associated with ~~that~~ the third port input;

switching data from the output of the second buffer memory to an input of the at least third buffer memory, and coupling an output of the at least third buffer memory to the first port output.

45. (Previously Presented) The method of claim 44 where data flows from the first port input through a first multiplexor, the first buffer memory, a second multiplexor, the second buffer memory, thence to the first port output.

46. (Previously Presented) The method of claim 44 where not all data follows same path through the buffer memories

47. (Previously Presented) The method of claim 43 where transmitting data from the second port is disabled in response to a command from a flow-control logic.

48. (Currently Amended) The method of claim 47 further comprising informing the flow-control logic how much space is available in the first buffer memory..

49. (Previously Presented) The method of claim 43 where the data is packet data.